Introduction:

Purpose:

In the field of machine learning, matrix multiplication is a fundamental operation that plays a crucial role in various algorithms and computations. However, traditional processors often struggle to efficiently execute matrix multiplication tasks due to their general-purpose nature. This inefficiency results in increased time consumption and hampers the overall performance of machine learning applications. Therefore, there is a pressing need for a specialized processor design that incorporates matrix multiplication as a core instruction and aims to decrease time consumption in machine learning.

Project scope:

Intellera is a groundbreaking project aimed at designing a RISC-V based processor with a customized instruction set architecture (ISA) that includes matrix multiplication instructions. The goal of Intellera is to address the performance bottleneck caused by conventional processors when executing matrix operations in machine learning algorithms. By enhancing the processor's capabilities and providing dedicated hardware acceleration for matrix Multiply-Accumulate (MAC) operations, Intellera aims to significantly reduce the time consumed in machine learning tasks.

Intellera proposes a novel approach to address the time consumption challenge in machine learning. The project focuses on designing a RISC-V based processor that features an extended instruction set architecture specifically tailored for matrix multiplication. By integrating dedicated hardware support for matrix MAC operations, Intellera can harness the parallel processing capabilities of the processor to accelerate matrix computations and reduce the overall execution time.

The project utilizes the knowledge of computer hardware and Risc-v Instruction Set for creating a customized instruction set and concept of systolic arrays implementation for accelerating the multiplication of matrix.

Overview:

**Overall Description:**

The project encompasses the development of a versatile RISC-V processor with the primary objective of accelerating matrix multiplication operations, a pivotal task within the domain of machine learning and scientific computing. The project's evolution began with the implementation of a single-cycle RISC-V processor using Vivado, establishing a solid foundation for subsequent enhancements. The immediate plan involves transitioning this processor into a highly efficient, pipelined architecture with five stages. This pipeline design aims to mitigate hazards and optimize the execution of RISC-V instructions, delivering improved throughput and performance. Beyond the processor core, a key innovation lies in the integration of a dedicated systolic array hardware architecture, meticulously designed to expedite matrix multiplication. This addition introduces a specialized matrix computation engine, effectively harnessing parallelism to dramatically reduce execution times for large-scale matrix operations.

**Product Perspective:**

In the realm of modern computing, the demand for high-performance processors tailored to specific computational tasks has intensified. The customized RISC-V processor represents an innovative response to this demand, offering a scalable and efficient solution for accelerating matrix multiplication operations. It stands at the intersection of hardware and software, where traditional RISC-V architecture is enhanced with a carefully crafted systolic array for matrix operations. This project is a testament to the adaptability and extensibility of the RISC-V ISA, providing a dedicated solution for a critical computation within machine learning workflows. It complements existing processors by offering superior matrix computation capabilities, making it an invaluable tool for a wide range of applications, including deep learning, data analytics, and scientific simulations.

**Product Functions:**

The customized RISC-V processor serves several vital functions, addressing the specific computational requirements of matrix multiplication within the context of machine learning and scientific computing. Its primary functions include:

1. Pipelined RISC-V Execution: The processor transitions from a single-cycle design to a highly efficient five-stage pipeline, reducing instruction latency and increasing overall throughput. This enhancement optimizes the execution of a broad spectrum of RISC-V instructions.

2. Hazard Mitigation: The pipeline design incorporates hazard detection and resolution mechanisms to handle data hazards, control hazards, and structural hazards, ensuring smooth instruction execution and maintaining data consistency.

3. Matrix Multiplication Acceleration: The project introduces a dedicated systolic array hardware architecture, capable of rapidly performing matrix multiplication operations. This function vastly improves the efficiency of matrix computations, significantly reducing execution times for machine learning algorithms.

4. FPGA Implementation: The processor, along with the systolic array, is designed for deployment on FPGA platforms, with a preference for the Nexys 4 FPGA board. FPGA implementation allows for hardware-level validation, real-time performance evaluation, and practical usability in embedded systems and edge computing scenarios.

5. Performance Evaluation: Extensive benchmarking and performance testing are conducted, comparing the customized RISC-V processor's performance in matrix multiplication tasks with that of standard processors. This function serves to quantify the speedup achieved by the specialized matrix computation engine.

By combining these functions, the customized RISC-V processor addresses the pressing need for efficient matrix multiplication within machine learning and scientific computing, offering enhanced performance, scalability, and adaptability for a wide range of applications.

Work Breakdown Structure:

1: Research

* Books
* CS-51 course by Berkeley
* Verilog crash course
* Merl implementation Videos

2-Implementaion:

* Basic ALU design
* Incorporating simple instruction
* Designing single cycle processor

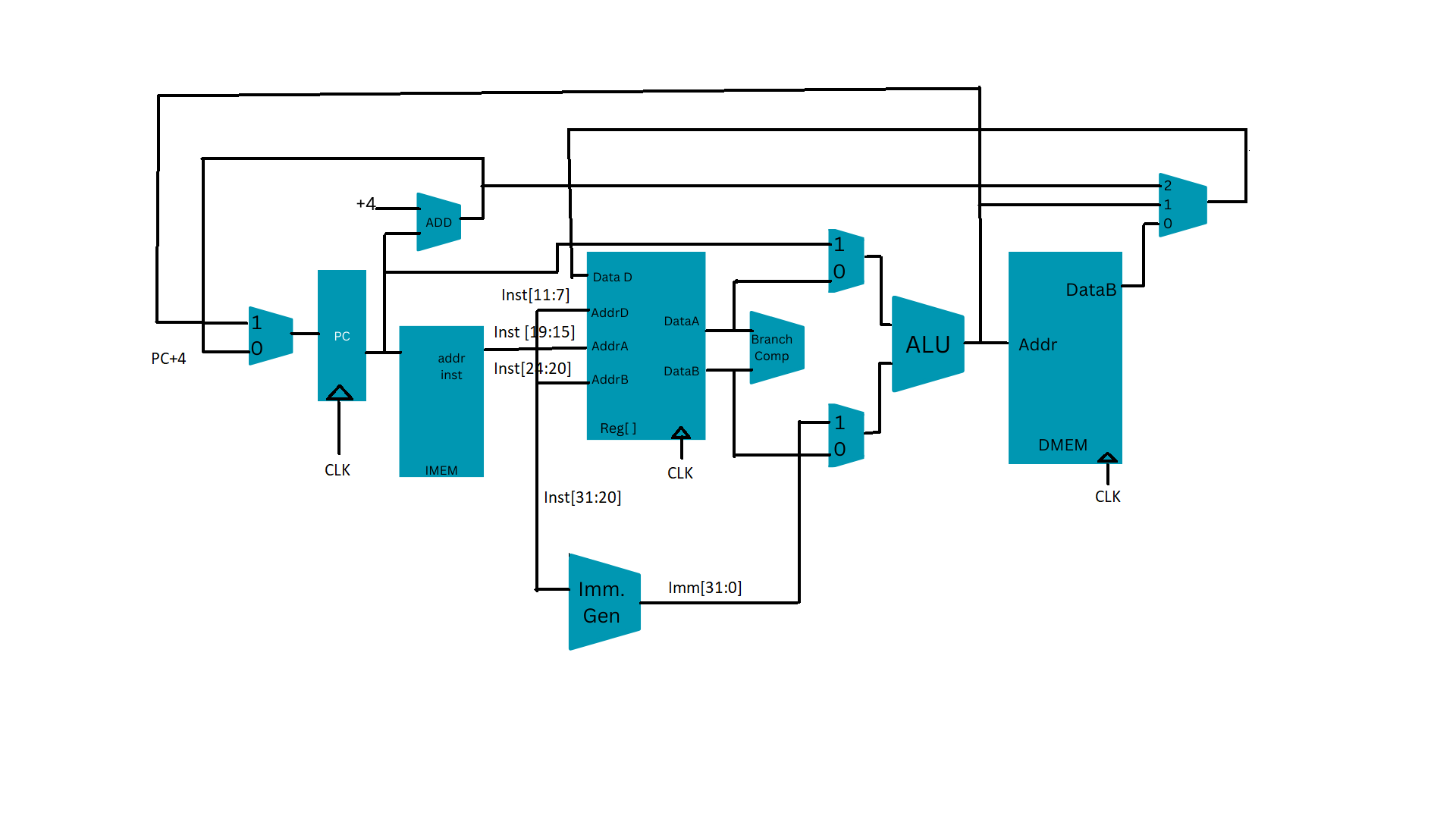
**Functional Requirements:**

* Custom ISA: The processor will support a custom instruction set architecture (ISA) optimized for matrix operations.
* Matrix Multiplication: The processor must efficiently execute matrix multiplication, meeting predefined performance benchmarks.
* Matrix Addition: It should also perform matrix addition precisely, adhering to specified computational requirements.
* Pipelining: Pipelining techniques should systematically be implemented within the RISC-V processor to enhance its performance and speed for matrix operations
* Instruction-level Parallelism: The processor must exploit ILP to execute multiple instructions simultaneously when applicable to matrix operations.
* FPGA Implementation: The processor and associated components must be compatible with FPGA implementation, leveraging its capabilities for hardware prototyping.

**Non-Functional Requirements:**

* Power Efficiency: The hardware must operate within defined power constraints, ensuring energy-efficient performance.
* Scalability: The processor should be designed to scale efficiently to accommodate various matrix sizes and complexities.
* Performance: The processor should meet or exceed established performance benchmarks in matrix operations.
* Compatibility: Where applicable, compatibility with existing software or systems will be maintained.

**Design :**

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Performance tests:

**Comparative Analysis:** The project should include a comprehensive comparative analysis between the performance of the customized RISC-V processor with matrix multiplication acceleration and a standard, non-accelerated RISC-V processor. This analysis will serve as a critical benchmark to demonstrate the efficiency gains achieved by the customized hardware. By writing the matrix multiplication code in assembly and executing it with the external systolic array implementation and with basic the Instruction set.the customized architecture should be faster.

**Documentation and Reporting:** Clear and thorough documentation of the hardware design, implementation details, and performance results is essential. The project should provide comprehensive reports detailing the methodology, test cases, and performance measurements for transparency and reproducibility.